

AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) A ferroelectric memory device comprising a plurality of
~~having plural~~ memory cells, each memory cell including ~~composed of~~ a respective memory cell
transistor and a respective memory cell capacitor, such that the ferroelectric memory device
includes a plurality of memory cell transistors and a plurality of memory cell capacitors, wherein

wherein each ~~said~~ respective memory cell capacitor comprises:

_____ a lower electrode ~~that is~~ connected to a bit line via the respective memory cell
transistor;

_____ a ferroelectric layer ~~that is~~ formed on an upper surface of the lower electrode and
~~has~~ having a width direction that is the same as a width direction of the lower electrode ~~as its~~
~~width direction~~; and

_____ an upper electrode ~~that is~~ formed on an upper surface of the ferroelectric layer and
~~has~~ having a width direction that is the same as the width direction of the lower electrode ~~as its~~
~~width direction~~,

wherein the ~~said~~ lower electrodes ~~electrode~~ of the respective memory cell capacitors
~~capacitor is~~ are independent from one another ~~for each of the memory cell capacitors~~,

wherein the ~~said~~ upper electrodes ~~electrode~~ of the respective memory cell capacitors
~~capacitor constitutes~~ form a continuous plate electrode covering the lower electrodes of that is
~~common to the plural~~ memory cell capacitors, and

wherein the width of ~~said~~ each respective upper electrode is narrower than the width of
the each respective ferroelectric layer.

Claim 2 (Currently Amended) The ferroelectric memory device as defined in Claim 1

wherein the width of ~~the~~ each respective lower electrode is narrower than the width of ~~the~~ each respective ferroelectric layer.

Claim 3 (Currently Amended) The ferroelectric memory device as defined in Claim 2

wherein the width of ~~the~~ each respective upper electrode and the width of ~~the~~ each respective lower electrode are substantially the same, and

wherein a ~~the~~ position of the each respective upper electrode in the width direction and ~~the~~ a position of the each respective lower electrode in the width direction are substantially aligned ~~aligns with each other~~.

Claim 4 (Currently Amended) The ferroelectric memory device as defined in Claim 2

wherein the width of ~~the~~ each respective upper electrode and the width of ~~the~~ each respective lower electrode are substantially the same, and

wherein a ~~the~~ position of the each respective upper electrode in the width direction and ~~the~~ a position of the each respective lower electrode in the width direction are different ~~from~~ each other.

Claim 5 (Currently Amended) A ferroelectric memory device comprising a plurality of

~~having plural~~ memory cells, each memory cell including ~~composed of a~~ respective memory cell

transistor and a respective memory cell capacitor, such that the ferroelectric memory device

includes a plurality of memory cell transistors and a plurality of memory cell capacitors, ~~wherein~~

wherein each ~~said~~ respective memory cell capacitor comprises:

_____ a lower electrode ~~that is~~ connected to a bit line via the respective memory cell

transistor;

 a ferroelectric layer ~~that is~~ formed on an upper surface of the lower electrode; and
 an upper electrode ~~that is~~ formed on an upper surface of the ferroelectric layer,
wherein the said lower electrodes-electrode of the respective memory cell capacitors are-
capacitor is independent from one another for each of the memory cell capacitors,

 wherein the said upper electrodes-electrode of the respective memory cell capacitors form
capacitor constitutes a continuous plate electrode covering the lower electrodes of that is-
common to the plural memory cell capacitors,

 wherein a position of one edge of the each respective upper electrode substantially aligns
with a position of one-an edge of the each respective ferroelectric layer, and

 wherein the other another edge of the each respective upper electrode is inwardly located
at-an inner a position-with relative to the another edge of each respective ferroelectric layer.

Claim 6 (Currently Amended) The ferroelectric memory device as defined in Claim 5
wherein one edge of each respective lower electrode is inwardly located at a position relative to
one edge of each respective upper electrode, and a position of another-one edge of the each
respective lower electrode substantially aligns with a position of another-one edge of the each
respective upper electrode.

Claim 7 (Currently Amended) A ferroelectric memory device comprising a plurality of-
having plural memory cells, each memory cell including-composed of a respective memory cell
transistor and a respective memory cell capacitor, such that the ferroelectric memory device
includes a plurality of memory cell transistors and a plurality of memory cell capacitors, wherein

wherein each said-respective memory cell capacitor comprises:

_____ a lower electrode ~~that is~~ connected to a bit line via the respective memory cell transistor;

_____ a ferroelectric layer ~~that is~~ formed on an upper surface of the lower electrode; and

_____ an upper electrode ~~that is~~ formed on an upper surface of the ferroelectric layer,

wherein the said lower electrodes ~~electrode~~ of the ~~respective~~ memory cell capacitors ~~are~~ capacitor is independent from one another ~~for each of the memory cell capacitors~~,

wherein the said upper electrodes ~~electrode~~ of the ~~respective~~ memory cell capacitors ~~capacitor constitutes~~ form a continuous plate electrode covering the lower electrodes of that is ~~common to the plural~~ memory cell capacitors,

wherein a position of one edge of ~~the~~ each respective upper electrode substantially aligns with a position of one ~~an~~ edge of ~~the~~ each respective ferroelectric layer,

wherein the other ~~another~~ edge of ~~the~~ each respective upper electrode is inwardly located at ~~an inner~~ a position ~~with~~ relative to another ~~the~~ edge of each respective ferroelectric layer, and

wherein one edge of ~~the~~ each respective lower electrode is inwardly located at ~~an inner~~ a position ~~with~~ relative to one edge of each respective ~~the~~ ferroelectric layer, and a position of another ~~the other~~ edge of ~~the~~ each respective lower electrode substantially aligns with a position of another ~~an~~ edge of ~~the~~ each respective ferroelectric layer.

Claim 8 (Currently Amended) The ferroelectric memory device as defined in Claim 1 wherein each respective ~~the~~ lower electrode ~~has~~ includes a groove-type structure.

Claim 9 (Currently Amended) The ferroelectric memory device as defined in Claim 8

wherein a groove formed in ~~the~~ each respective lower electrode extends along a direction that is parallel to ~~the~~ a direction along which ~~the~~ each respective upper electrode extends.

Claim 10 (Currently Amended) The ferroelectric memory device as defined in Claim 8 wherein a direction along which ~~the~~ a groove formed in ~~the~~ each respective lower electrode extends is perpendicular to a direction along which ~~the~~ each respective upper electrode extends.

Claim 11 (Currently Amended) A ferroelectric memory device comprising a plurality of ~~having plural~~ memory cells, each memory cell including ~~composed of~~ a respective memory cell transistor and a respective memory cell capacitor, such that the ferroelectric memory device includes a plurality of memory cell transistors and a plurality of memory cell capacitors, wherein

wherein each ~~said~~ respective memory cell capacitor comprises:

_____ a lower electrode ~~that is~~ connected to a bit line via the respective memory cell transistor;

_____ a ferroelectric layer ~~that is~~ formed on an upper surface of the lower electrode; and

_____ an upper electrode ~~that is~~ formed on an upper surface of the ferroelectric layer,

wherein the ~~said~~ lower electrodes ~~electrode~~ of the respective memory cell capacitors are ~~capacitor is an electrode having a groove-type structure that is independent from one another for each memory cell capacitor, and~~

wherein an interlayer insulating film is formed over each respective lower electrode,

wherein a respective groove is formed on the interlayer insulating film formed over each respective lower electrode so as to cover each respective lower electrode, and

wherein the ~~said~~ upper electrode of the each respective memory cell capacitor is formed

in the respective groove and on a circumference area of the respective groove, and forms-
~~constitutes~~ a continuous plate electrode covering the lower electrodes of ~~that is common to the~~
~~plural~~ memory cell capacitors.

Claim 12 (Currently Amended) The ferroelectric memory device as defined in Claim 11
wherein ~~a~~ the respective groove formed ~~in~~ on the interlayer insulating film formed over the each
respective lower electrode extends along a direction that is parallel to ~~the~~ a direction along which
~~the each respective~~ upper electrode extends.

Claim 13 (Cancelled)

Claim 14 (Currently Amended) The ferroelectric memory device as defined in Claim 11
wherein ~~the each respective~~ lower electrode ~~having the groove-type structure~~ comprises:
a first lower electrode section ~~in~~ having a planar shape forming ~~that constitutes~~ a bottom
part of the respective groove; ~~and;~~ and
a second lower electrode section forming ~~that constitutes~~ side surface parts and
circumference parts of the respective groove.

Claim 15 (Currently Amended) The ferroelectric memory device as defined in Claim 11
wherein ~~the each respective~~ lower electrode ~~having the groove-type structure~~ comprises:
a first lower electrode section ~~that constitutes~~ forming a bottom part of the respective
groove; and
a second lower electrode section ~~that constitutes~~ forming only side surface parts of the

respective groove.